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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/798,943	03/12/2004	Jong-Joo Lee	25611-000080/US	6887
30593	7590	05/05/2005	EXAMINER	
HARNESSE, DICKEY & PIERCE, P.L.C.			SANDVIK, BENJAMIN P	
P.O. BOX 8910			ART UNIT	
RESTON, VA 20195			PAPER NUMBER	
			2826	

DATE MAILED: 05/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/798,943

Applicant(s)

LEE, JONG-JOO

Examiner

Ben P. Sandvik

Art Unit

2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-17 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-17 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
- 1) ☒ Certified copies of the priority documents have been received.
  - 2) ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- |                                                                                                    |                                                                             |
|----------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                        | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)               | Paper No(s)/Mail Date. ____.                                                |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date ____.                                                                        | 6) <input type="checkbox"/> Other: ____.                                    |

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-3, 7, 9-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Corisis et al (U.S. PG Pub #20010040282), in view of Cady et al (U.S. Patent #6576992).

With respect to **claims 1-3, 7, 9-16**, Corisis teaches at least two packages of area array type disposed to form a stack (Fig. 1), each package including: a substrate having a first face and second face opposing the first face (Fig. 1, 12), there being a plurality of terminal pads (Fig. 9, 20) and a plurality of connecting pads (Fig. 9, 28) formed on the second face, and a semiconductor chip (Fig. 1, 14) attached to the first face of the substrate and electrically connected (Fig. 1, 22) to the terminal pads and the connecting pads,

that the semiconductor chip is a center pad type chip (Fig. 9),

a first wirings providing electrical paths coupling the semiconductor chip and the terminal pads (Fig. 9, 22), and a second wirings providing electrical paths coupling the semiconductor chip and the connecting pads (Fig. 9, 30),

connecting pads arranged in a straight row near an edge of the substrate (Fig. 9, 28),

a plurality of external connection terminals formed on the terminal pads of a lowermost package of the packages (Fig. 1, 28 and Paragraph 26),

each array type package is a ball grid array package (Paragraph 9),

the first wirings are formed on the second face of the substrate (Fig. 1, 22)

Corisis does not teach at least one flexible cable having a plurality of conductive patterns thereon extending around at least one side edge of a lower one of the at least two packages, and electrically coupling the connecting pads of the packages through the conductive patterns, or that the package further comprises a non-conductive adhesive layer interposed between adjacent lower and upper packages.

Cady teaches a flexible circuit having a plurality of conductive patterns thereon extending around at least one side edge of a lower one of the at least two packages, and electrically coupling the connecting pads of the packages through the conductive patterns (Fig. 1, 32), and a non-conductive adhesive layer interposed between adjacent lower and upper packages (Fig. 1, 34). It would have been obvious to one of ordinary skill in the art at the time the invention was made to connect the packages of Corisis using the flexible circuit of Cady in order to make a compact stacked package for high-density modules, and to

interpose a an adhesive layer between adjacent lower and upper packages as taught by Cady in order to enhance the mechanical strength of the package.

Claims 4-6, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Corisis and Cady, further in view of Kim et al (U.S. Patent #20020043702).

With respect to **claims 4-6 and 17**, Corisis and Cady teach all of the limitations of claim 1, and furthermore Corisis teaches

a first wirings providing electrical paths coupling the semiconductor chip and the terminal pads (Fig. 9, 22), and a second wirings, including vias (Fig. 3, 34), providing electrical paths coupling the semiconductor chip and the connecting pads (Fig. 9, 30),

the vias are located in immediate proximity to the connecting pads (Fig. 3, 34 and 32),

the first wirings are arranged on the first face of the substrate (Fig. 6, 22) and the second wirings are arranged on the second face of the substrate (Fig. 4, 30).

Corisis and Cady do not teach that the semiconductor chip is an edge pad type chip. Kim teaches a BGA package comprising a semiconductor chip connected to a substrate using edge bonding (Fig. 6b). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use edge pad bonding in the package of Corisis and Cady based on the teachings of Kim in order to reduce the length of the bonding wire.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Corisis and Cady, further in view of Rolda et al (U.S. PG Pub #20020030261).

With respect to **claim 8**, Corisis and Cady teach all of the limitations of claim 1, but do not teach connecting pads arranged in a staggered row near an edge of the substrate. Rolda teaches that solder balls can arranged in a staggered pattern (Paragraph 43). It would have been obvious to one of ordinary skill in the art at the time the invention was made to arrange the connecting pads of Corisis in a staggered pattern according to the teachings of Rolda in order to reduce the thermomechanical stresses in the package.


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ben P. Sandvik whose telephone number is (571) 272-8446. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2826

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

bps



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